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Remarks:

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Status of Claims

Claims 1 – 43 are pending in the application. Claims 1 – 23 and 27 – 43 have been rejected.

Claims 24 – 26 have been canceled without prejudice or disclaimer. In making this cancellation without prejudice, Applicants reserve all rights in these claims to file continuation or divisional patent applications.

Voluntary Claim Amendments

Claims 1-5, 7-10, 12-23, and 27-43 have been amended voluntarily to more clearly claim that which the inventors regard as their invention. These amendments do not add new matter. These amendments are not being made for reasons of patentability and do not narrow the scope of the claims. For example, the acronym 'ALU' was replaced with the phrase -- arithmetic logic unit--. In another example, 'storing' was replaced with --to store-- and 'stores' was replaced with --is to store--. In a further example, all occurrences of the term 'cycles' were replaced with --clock cycles--.

Drawings

Applicants note that formal drawings will be required when the application is allowed.

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35 U.S.C. 112 Rejections

The Office Action rejects claims 2, 3, 8 – 23, 28, 39 – 43 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Office Action stated that regarding claims 2, 3, 19, 20, 28, 39 and 40, “the variable ‘N’ stated in the claims is not defined. Additional information is required”.

Claims 2, 3, 19, 20, 28, 39 and 40 have been amended to delete any reference to the variable ‘N’, thus overcoming the rejection.

The Office Action stated that regarding claims 23 and 43, “the variables ‘P’ and ‘L’ stated in the claims are not defined. Additional information is required”.

Claims 23 and 43 have been amended to include definitions of the variables ‘P’ and ‘L’, thus overcoming the rejection. Support for the amendments to claims 23 and 43 may be found on page 22 of the instant application.

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35 U.S.C. 102 Rejections

The Office Action rejects claims 1 – 23 and 27 – 43 under 35 U.S.C. 102(e) as being anticipated by Baek (US 6,084,925). Applicants respectfully traverse the rejection, in view of the remarks that follow.

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” (MPEP 2131)

Claim 27 recites *“generating a series of trace bits; and storing a first half of said series sequentially in a first register and a second half of said series sequentially in a second register.”*

Baek does not disclose, either expressly or inherently, all the limitations of claim 27. Baek makes no mention whatsoever of how trace bits are stored in trace-back registers 42, 43, 44 and 45, and in particular, makes no mention of whether the trace bits are stored sequentially or otherwise in the trace-back registers. Moreover, Baek does not teach, either expressly or inherently, *“storing a first half of said series ... in a first register and a second half of said series ... in a second register”*. Rather, each of the trace-back registers 42, 43, 44 and 45 stores “survival paths corresponding to the respective initial state”.

Therefore, Baek cannot anticipate claim 27. Claims 28 – 38 are dependent from claim 27 and include all the limitations of the independent claim. Therefore, Baek does not disclose, either expressly or inherently, all the limitations of claims 28 – 38 and cannot anticipate claims 28 – 38.

Claim 1 as amended recites *“a first register and a second register to jointly store at most a single copy of said trace bits”*.

Baek does not disclose, either expressly or inherently, all the limitations of claim 1. Rather, Baek discloses trace-back registers 42, 43, 44, and 45 that each store a single copy of trace bits. Jointly, trace-back registers 42, 43, 44 and 45 store four copies of the trace bits.

Therefore, Baek cannot anticipate claim 1 as amended. Claims 2 – 18 are dependent from claim 1 and include all the limitations of the independent claim. Therefore, Baek does

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not disclose, either expressly or inherently, all the limitations of claims 2 – 18 and cannot anticipate claims 2 – 18.

Claim 19 as amended recites "*a first register and a second register to jointly store a single copy of trace bits of at least a portion of one stage*".

Baek does not disclose, either expressly or inherently, all the limitations of claim 19. Rather, Baek discloses trace-back registers 42, 43, 44 and 45 that each store a single copy of trace bits. Jointly, trace-back registers 42, 43, 44 and 45 store four copies of the trace bits.

Therefore, Baek cannot anticipate claim 19 as amended. Claims 20 – 23 are dependent from claim 19 and include all the limitations of the independent claim. Therefore, Baek does not disclose, either expressly or inherently, all the limitations of claims 20 – 23 and cannot anticipate claims 20 – 23.

Claim 39 as amended recites "*storing a single copy of trace bits of at least a portion of one stage jointly in a first register and a second register*".

Baek does not disclose, either expressly or inherently, all the limitations of claim 39. Rather, Baek discloses trace-back registers 42, 43, 44 and 45 that each store a single copy of trace bits. Jointly, trace-back registers 42, 43, 44 and 45 store four copies of the trace bits.

Therefore, Baek cannot anticipate claim 39 as amended. Claims 40 – 43 are dependent from claim 19 and include all the limitations of the independent claim. Therefore, Baek does not disclose, either expressly or inherently, all the limitations of claims 40 – 43 and cannot anticipate claims 40 – 43.

The Office Action states "regarding claims 2-11 and 28-31, the trace bits are stored in the shift registers and input into the trace back memory (figures 2 and 4)". Applicants strongly disagree with this statement. At col. 2, lines 50 – 61, Baek discloses: "Referring to FIG. 2, a convolutional encoder for producing a convolutional code (at the transmission side) is illustrated. An input information bit is supplied from an input terminal to a shift register consisting of bit registers SR1 and SR2. A total of three bits consisting of the input information bit and previous information bits, respectively stored in the registers SR1 and SR2, are supplied to an exclusive-OR gate and an exclusive OR of the respective bits is

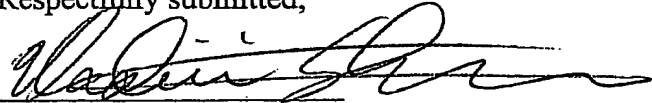
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calculated. On the other hand, the input information bit and the information bit stored in the register SR2 are supplied to an exclusive OR-gate and an exclusive OR of these information bits is also calculated." Baek does not disclose, either expressly or inherently, storing trace bits in the shift registers SR1 and SR2 of Figure 2.

Moreover, the meaning of the term "cycle" in Baek is similar to the meaning of the term "stage" in the instant application.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,



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